

# 8\*8 Bit low Power High Speed Multiplier

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**ABSTRACT:**The need of portable devices like mobile phones and laptops is the low power circuits and delay being the important criteria for the performance evaluation of any digital circuit is the challenge for designers .So, in this paper a low power high speed 8\*8 bit multiplier has been designed using the 4\*4 bit multiplier circuit.The design of various 8\*8 bit multiplier has been designed in virtuoso platform .The delay and power parameters are improved in various multiplier circuits.

**Keywords:** Low power, Wallace Tree, Array ,Compressor

**INTRODUCTION:**The most important block in calculating the speed of the processor is multiplier in DSP and other applications. To find the speed of the processor the speed of the multiplier is observed .The multiplier comprises of an And gate and the adder circuit .And gate to generate the partial products and the adder circuit to add the partial products. Further various methods are adopted by various authors to speed up the adder procedure or to improve the delay parameter of the multiplier such as Array multiplier, Wallace Tree multiplier and compressor (n:2 ) counter multiplier.To decrease the power , low power gates and circuits are designed and used in the multiplier circuit . As the generation of partial products are obtained by And gates, so a low power And gate has been designed and used. The next step in the multiplier is to add the generated partial products . To reduce the delay fast adders has been designed .Various fast adders are designed has been used to obtain the product. The multiplier are widely used in DSP ,filter.

## RELATED WORK

4\*4 bit multiplier circuit: The first step in the multiplier is to generate the partial product which is obtained using the And gate . Where as the And gate is designed using the transmission gate technology. The transmission gate technology is applied to obtain the reduced power consumption or to improve the delay parameter. The second step in any multiplier architecture is to add the generated partial products . The addition may be done by using various addition arrangements such as Ripple Carry Adder, Carry Select Adder. To speed up the multiplier the multiplier architecture such as Array , Wallace Tree and n:2 Compressor multiplier has been used . Adder is And gate and . Array multiplier being the simple and regular structure is used where as the delay is increased as the no of bits in a multiplier is increased . The delay in Wallace tree and n:2 compressor is better as compared to the array multiplier architecture . The adder circuit has been designed using the transmission gate technology to reduce the power and to improve the speed the multiplier architecture is chosen as per the application. the example of multiplier is as shown in the figure 1

$$\begin{array}{r}
 10001011 \\
 01010011 \\
 \hline
 10001011 \quad \text{PP1} \\
 10001011 * \quad \text{PP2} \\
 00000000 ** \quad \text{PP3} \\
 00000000 *** \quad \text{PP4} \\
 10001011 **** \quad \text{PP5} \\
 00000000 ***** \quad \text{PP6} \\
 10001011 ***** \quad \text{PP7}
 \end{array}$$

00000000\*\*\*\*\*

PP8

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$P_{15}P_{14}P_{13}P_{12}P_{11}P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$  (result)

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Figure1: 8 \* 8 Bit Multiplier Example

The partial products PP1 to PP8 are generated using And gate.where as the result  $P_0$  to  $P_{15}$  are obtained using the 1 - bit adder circuit .The 1- bit adder has been designed using the transmission gate technology in which the 28 transistors are used and using 32 transistors in conventional adder circuit. The 4\*4 bit multiplier circuit has been designed using the above mentioned designed And gate and adder circuit.further the Array , Wallace Tree and n:2 compressor architecture has been designed .

Array Architecture: The array architecture is simple and regular in structure. The Array architecture is using two input AND  $x*y$  gate to generate the partial products and n-1 ,y bit adder.

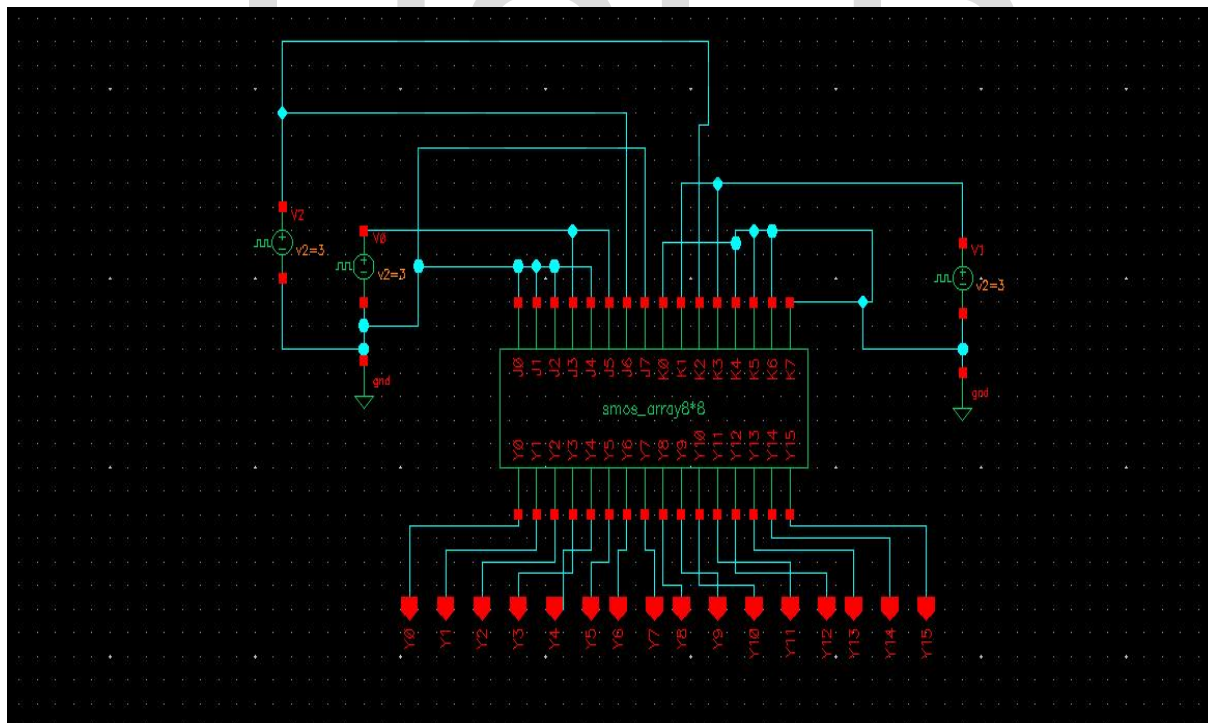


Figure 2 : 8\*8 Bit Array Multiplier Using Conventional Multiplier

Wallace Tree Architecture : C.S Wallace proposed the Wallace Tree multiplier in 1964 that can handle the multiplication process for large operands .To reduce the

number of partial products Wallace Tree is the better option .The over all delay is proportional to  $(\log_{3/2} n)$  for n number of rows .The Wallace tree architecture using the conventional multiplier is shown in figure 3.

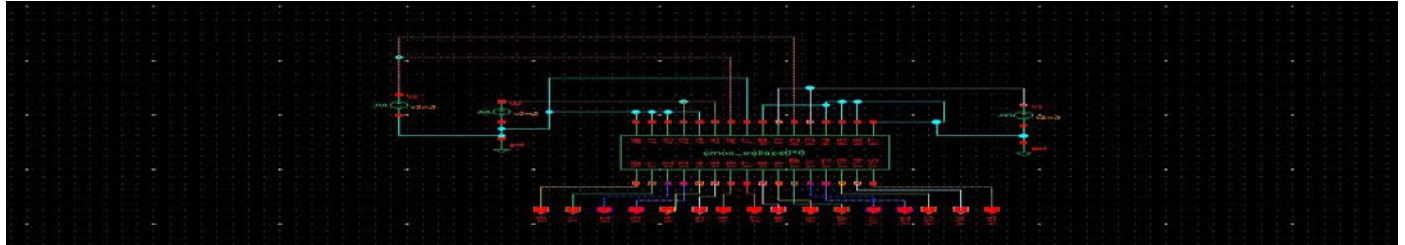


Figure 3 8\*8 Bit Wallace Tree Multiplier Using Conventional Multiplier

Proposed Multiplier : Here the 8\*8 bit multiplier is proposed using the 4\*4 bit multiplier unit , where as the 4\*4 bit multiplier has been designed using their conventional 32 transistor adder and the 28 transistor adder circuit.The multiplier architectures discussed above has been designed as discussed..

8\*8 multiplier using 4\*4 multiplier: Let the multiplier and the multiplicand be  $A_{7-0}$  and  $B_{7-0}$  and  $P_{15-0}$  be the resultant product .  $A_{7-0}$  is partitioned into two groups as  $A_{7-4}$  and  $A_{3-0}$  similarly  $B_{7-0}$  is partitioned to two groups as  $B_{7-4}$  and  $B_{3-0}$  .the resultant 16 bit product is obtained as shown in figure 4.

$$\begin{array}{r}
 A_{7-4} \quad A_{3-0} \\
 B_{7-4} \quad B_{3-0} \\
 \hline
 A_{3-0} * B_{3-0} \qquad \qquad \qquad PP0 \\
 A_{7-4} * B_{3-0} \qquad \qquad \qquad PP1 \\
 A_{3-0} * B_{7-4} \qquad \qquad \qquad PP2 \\
 A_{7-4} * B_{7-4} \qquad \qquad \qquad PP3 \\
 \hline
 P_{15-12} \quad P_{11-8} \quad P_{7-4} \quad P_{3-0}
 \end{array}$$

Figure 4 Proposed 8\*8 Bit Multiplication Method

The final product bits i.e  $P_{15-12}$ ,  $P_{11-8}$ ,  $P_{7-4}$  and  $P_{3-0}$  are computed as shown below.

$$P_{15-12} = PP3_{7-4}$$

$$P_{11-8} = PP1_{7-4} + PP2_{7-4} + PP3_{3-0}$$

$$P_{7-4} = PP0_{7-4} + PP1_{3-0} + PP2_{3-0}$$

$$P_{3-0} = PP0_{3-0}$$

so the designed 4\*4 bit multiplier used to obtain the 8\* 8 bit resultant product.in the similar way the higher bit multiplier can be obtained. The figure 5,6 and 7 shows the blocks of proposed Array ,Wallace Tree and compressor based proposed multipliers

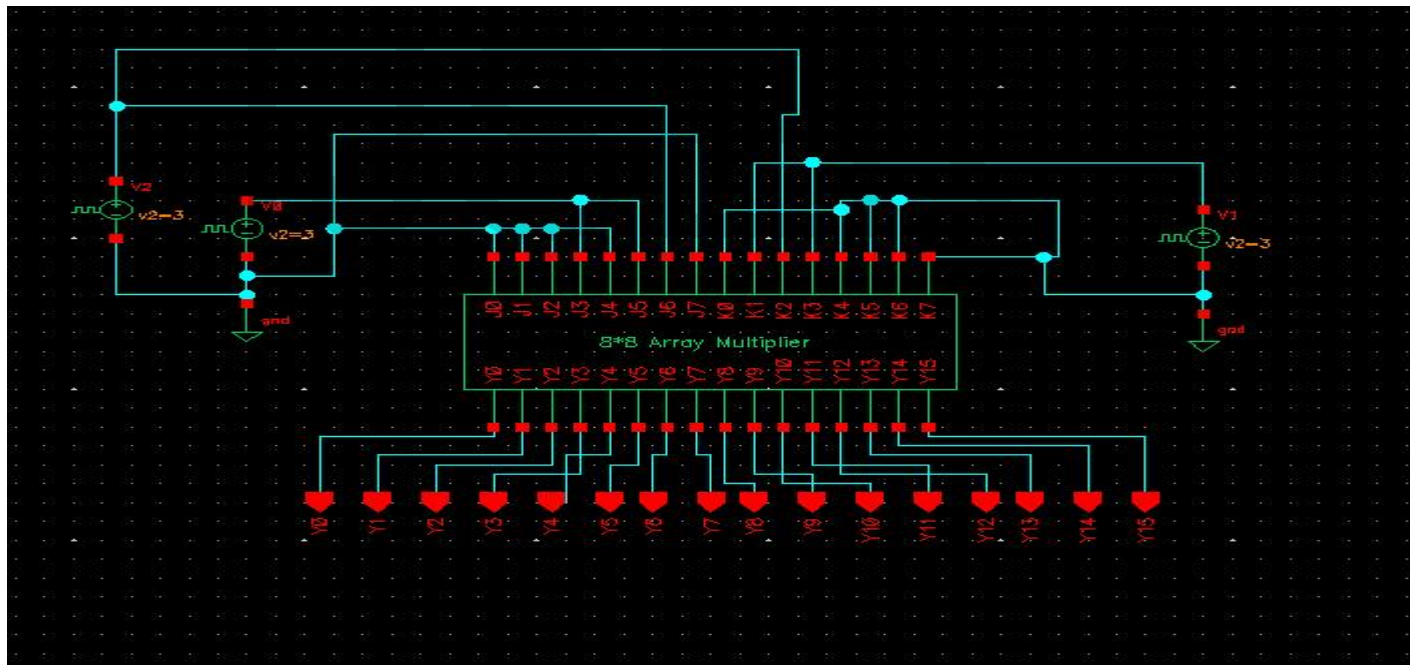


Figure 5 8\*8 Bit Array Proposed Multiplier

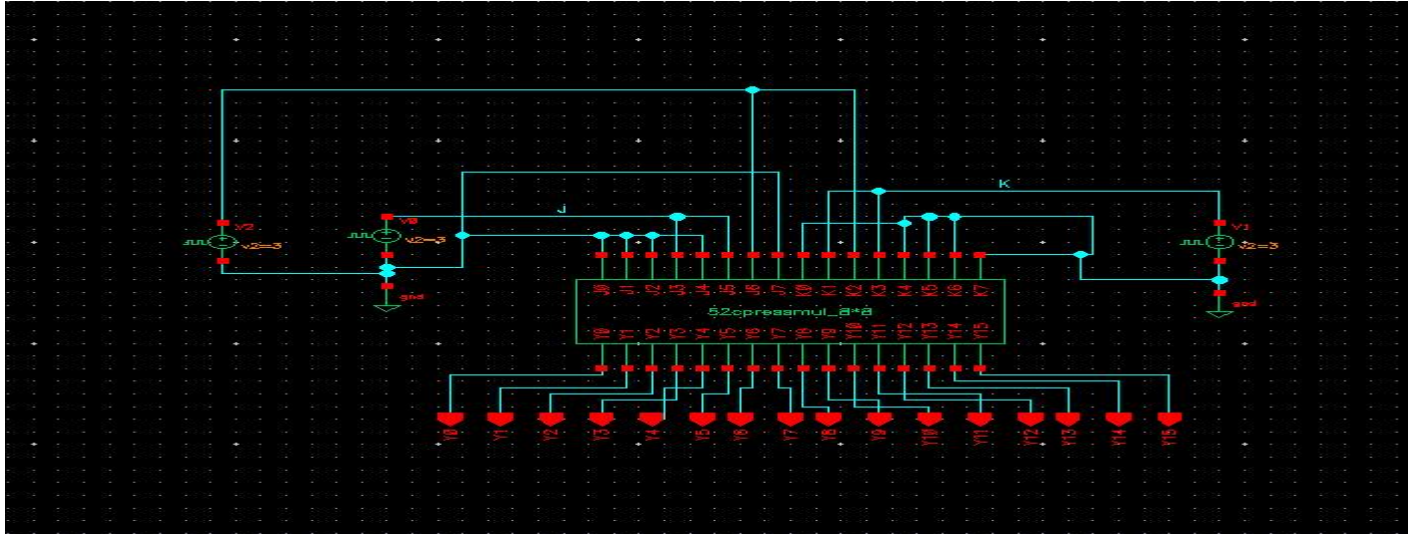


Figure 6: 8\*8 Bit 5:2 Compressor Proposed Multiplier

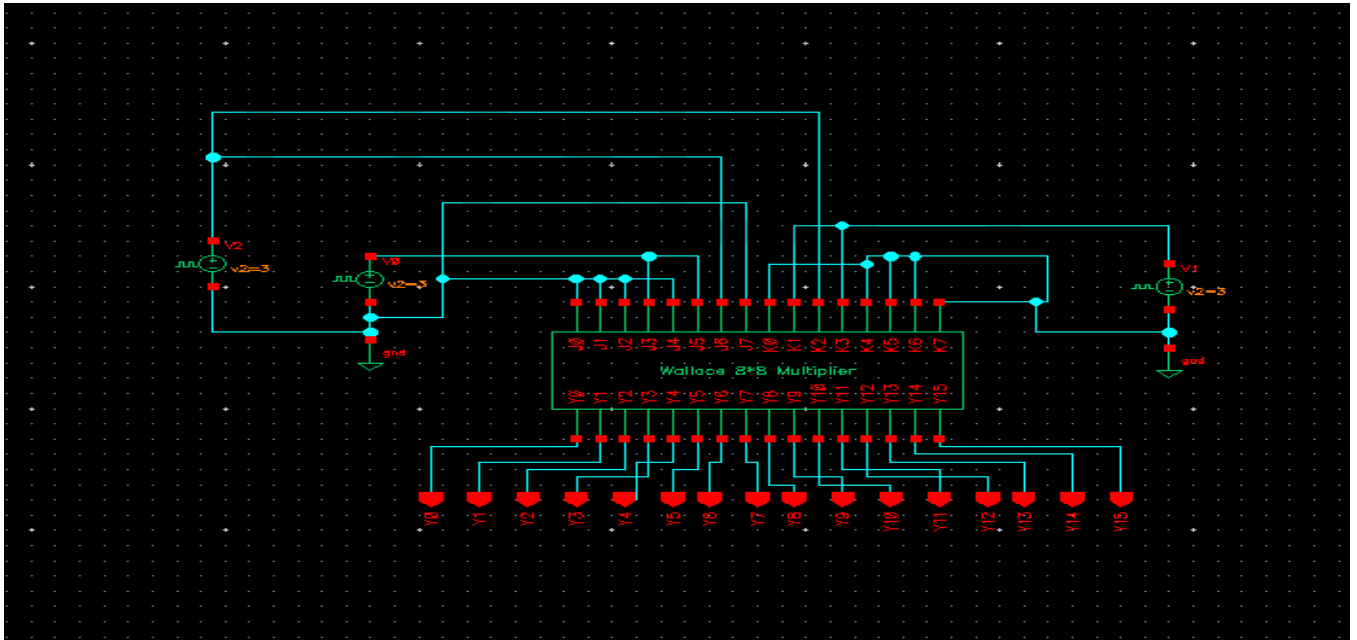


Figure 7 : 8\*8 Bit Wallace Tree Proposed Multiplier

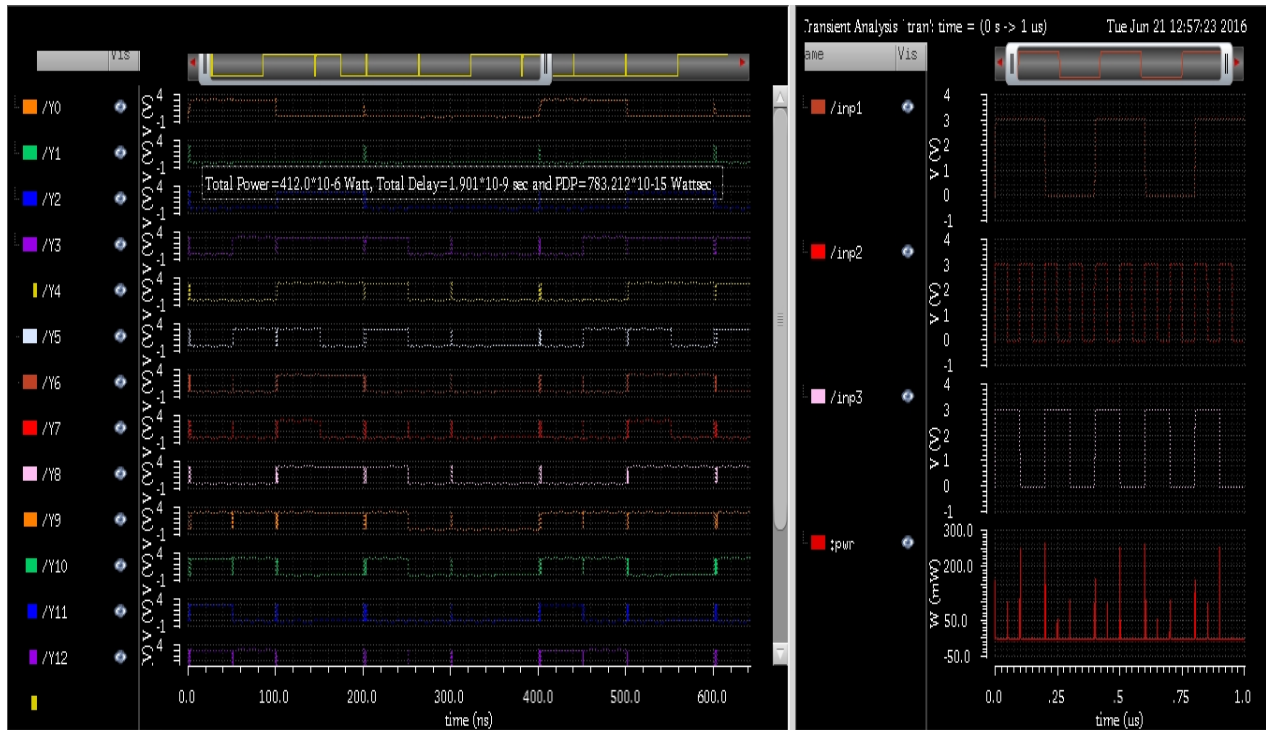


Figure 8: Output Waveform of 8\*8 Bit Proposed Array Multiplier

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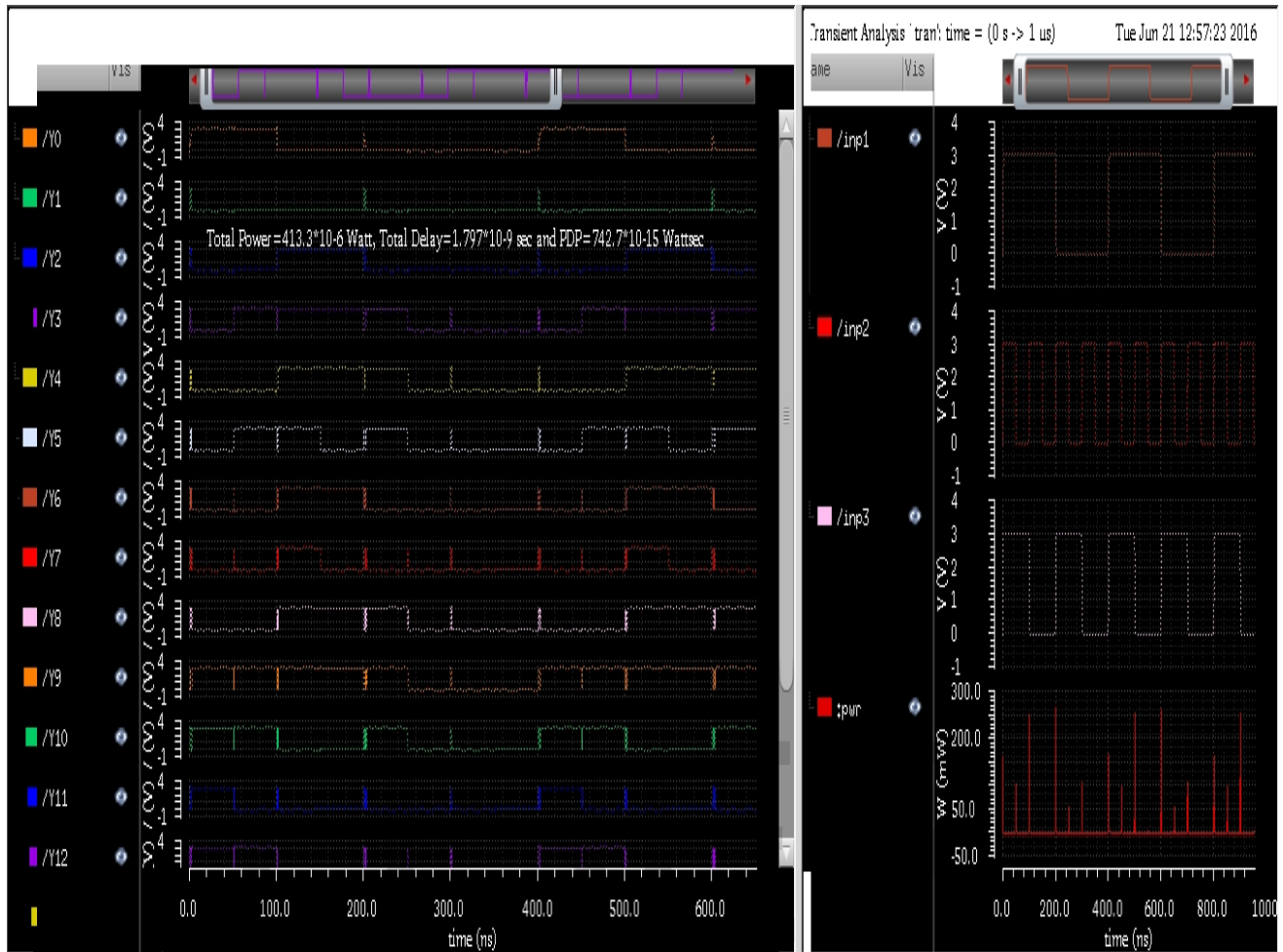


Figure 9: Output Waveform of 8\*8 Bit Proposed Wallace Tree Multiplier

Simulation and Results: The 8\*8 bit multipliers has been designed using the cadence Virtuoso and various parameters such as delay and power is obtained. The Array ,Wallace Tree and n:2 compressor multiplier architecture has been designed and compared . The output waveform shown in figure 8 and figure 9 verifies the functionality of the proposed Array and Wallace Tree multiplier circuit. The conventional array multiplier have a PDP of 1678.179 Watt sec where as the proposed array multiplier of 783.212 Watt sec The conventional Wallace Tree multiplier have a PDP of 1503.4281Watt sec where as the proposed Wallace Tree multiplier of 783.212 Watt sec .The conventional Compressor multiplier have a PDP of 1758.736 Watt sec where as the proposed Compressor multiplier



have PDP of 746.149 Watt sec. Table 1 shows the comparison of conventional and proposed multipliers

Table1: Comparison Table of 8\*8 Bit Multipliers

Sr. No	Multipliers/ Parameters	Conventional		Proposed		PDP	
		Delay n sec	Power $\mu$ watt	Delay n sec	Power $\mu$ watt	Conventional Watt sec $*10^{-15}$	Proposed Watt sec $*10^{-15}$
1	8*8 bit Array multiplier	3.09	543.1	1.901	412.0	1678.179	783.212
2	8*8 bit Wallace Tree multiplier	2.749	546.9	1.797	413.3	1503.4281	740.2203
3	8*8 bit compressor multiplier	3.064	574.0	1.73	431.3	1758.736	746.149

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